



10-Bit, Integrated, Multiformat SDTV/HDTV Video Decoder and RGB Graphics Digitizer

ADV7181C

TIMING CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
UPDATED SPECIFICATION						
Data Output Transition Time DDR (CP) ¹	t ₁₅	Positive clock edge to end of valid data	1.9			ns
Data Output Transition Time DDR (CP) ¹	t ₁₆	Start of valid data to positive clock edge	1.7			ns
Data Output Transition Time DDR (CP) ¹	t ₁₇	Negative clock edge to end of valid data	1.4			ns
Data Output Transition Time DDR (CP) ¹	t ₁₈	Start of valid data to negative clock edge	1.7			ns
ORIGINAL SPECIFICATION						
Data Output Transition Time DDR (CP) ²	t ₁₅	Positive clock edge to end of valid data	−4 + TLLC/4			ns
Data Output Transition Time DDR (CP) ²	t ₁₆	Positive clock edge to start of valid data	0.25 + TLLC/4			ns
Data Output Transition Time DDR (CP) ²	t ₁₇	Negative clock edge to end of valid data	−2.95 + TLLC/4			ns
Data Output Transition Time DDR (CP) ²	t ₁₈	Negative clock edge to start of valid data	−0.5 + TLLC/4			ns

¹ Guaranteed by characterization up to 75MHz pixel clock.

² DDR timing specifications dependent on LLC output pixel clock; TLLC/4 = 9.25 ns at LLC = 27 MHz.